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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,175	05/03/2001	Sang Hoo Dhong	AUS920010087US1	7651

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,175	DHONG ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 The application of Dhong et. al. entitled COMMUNICATION BUS WITH REDUNDANT SIGNAL PATHS AND METHOD FOR COMPENSATING FOR SIGNAL PATH ERRORS IN A COMMUNICATION BUS filed on 5/3/2001 was examined. Claims 1-22 are pending.

Claim Rejections - 35 USC § 102

2.0 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, 11, 13-16 are rejected under 35 U.S.C. 102(B) as being anticipated by Atac (U.S. Patent No.: 4,985,830).

Referring to Claim 1, The reference teaches: a source node (PROCESSOR) connected via a source switching arrangement (BUS SWITCH) which is connected via alternate transmission paths (plurality of BRANCH BUS paths) to a destination switch (Another BUS SWITCH) to a destination node (Another PROCESSOR) per Fig 1.

The reference teaches that the BUS SWITCH is a card that is connected to the back plane per col. 2 lines 26-63 which is a common substrate as disclosed in the specification per col. 4 lines 12-21

In Addition the Primary Reference Teaches:

Regarding Claim 2, A plurality of BUS SWITCHES (multiple source switch devices) are connected to different PROCESSORS (sources) and at least one BUS SWITCH (destination switch device) is connected between the PROCESSOR (Destination node) and a plurality of BRANCH BUS (alternate transmission path) per Fig 1.

Regarding Claim 3, A BUS SWITCH (source switching device) performs as a multiplexer and another BUS SWITCH (destination switching device) performs as a multiplexer per Fig 1.

Regarding Claim 4, A BUS SWITCH (source switching device) performs as a switch control structure and another BUS SWITCH (destination switching device) performs as a switch control structure per Fig 1.

Regarding Claim 5, The BUS SWITCH performs the switch control function. A BUS SWITCH is inherently controlled by a BUS SWITCH CONTROLLER and a BUS SWITCH CONTROLLER is a processor which inherently contains memory.

Regarding Claim 8, The primary reference teaches plurality source PROCESSORS which are source and additional processors and a plurality of destination processors which are destination and additional processor with a plurality of BRANCH BUS connections between the source processor and additional source processor and destination and additional destination PROCESSORs (plurality of ALTERNATE paths). The BUS SWITCH which performs source switch arrangement and a BUS SWITCH which performs destination switch arrangement that can selectively connect and disconnect between the plurality of BRANCH BUS in order to provide transmission paths per Fig 1.

Regarding Claim 11, the plurality of BRANCH BUS can be divided up into subsets of alternate paths per Fig 1.

Referring to Claim 13, the reference teaches: a plurality of PROCESSOR (source nodes) are connected via a plurality of BRANCH BUS (communications bus) to a plurality of PROCESSOR (destination nodes) per Fig 1. There are a plurality of BRANCH BUS to provide alternate paths. The BUS switch performs the source switching arrangement and another BUS SWITCH performs a destination switch arrangement as shown in Fig 1. The BRANCH BUS provide a number of alternate transmission paths extending between each PROCESSOR (Source) and a matched destination node (PROCESSOR). The BUS SWITCHs set up a BRANCH BUS path which matches the PROCESSOR (source) to the PROCESSOR (destination) as shown per Fig 1.

The reference teaches that the BUS SWITCH is a card that is connected to the back plane per col. 2 lines 26-63 which is a common substrate as disclosed in the specification per col. 4 lines 12-21

In Addition the Primary Reference Teaches:

Regarding Claim 14, a BUS SWITCH (source switching devices) performs as a multiplexer and another BUS SWITCH (destination switching device) performs as a multiplexer per Fig 1.

Regarding Claim 15, A plurality of PROCESSORs or source nodes are connected side by side to the BUS SWITCH which is a common multiplexer as shown in Fig 1.

Regarding Claim 16, the plurality of BRANCH BUS can be divided up into subsets of alternate paths per Fig 1.

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atac et. al. (U.S. Patent No.4,985,830)

Referring to Claims 9, Atac teaches: the BUS SWITCH performs a source switching arrangement multiplexing function per Fig 1.

Atac does not expressly call for: source switching arrangement comprising a number of multiplexers but teaches multiplexing between a plurality or PROCESSORS per Fig 1.

It would have been an obvious to one of ordinary skill in the art at the time of the invention for the BUS SWITCH to comprise a number of multiplexers in order for the BUS SWITCH to multiplex between a plurality of PROCESSORs.

In Addition Atac teaches:

Regarding Claim 10, A plurality of PROCESSORs or source nodes are connected side by side to the BUS SWITCH which is a common multiplexer as shown in Fig 1.

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atac et. al. (U.S. Patent No.4,985,830) in view of Mostashari (U.S. Patent No.: 4,964,120)

Referring to Claim 6, The primary reference teaches: the communications bus of claim 1 and a source and destination node.

The primary reference does not expressly call for: applying a test signal to each alternate transmission path and for monitoring the destination node to determine whether the respective test signal is properly received at the destination node

Mostashari teaches: signals are applied to both cables between the two TBC modules or source and destination nodes per col. 2 lines 5-44 (Applying); A determination is made whether a valid signal received per col. 2 lines 5-44 (determining); If the same signal is not received then the TBC switch to an alternate cable (If test not properly received then switch paths)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the testing of a bus coupled between two electronic devices of Mostashari to the system of the primary reference in order to determine if there is a fault or failure in the path.

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 12 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atac (U.S. Patent No.: 4,985,830) in view of Wang (U.S. Patent No.; 6,188,271)

Referring to Claim 7, The primary reference teaches the communications bus of claim 1 and a receive PROCESSOR (destination node) wherein the input of the Receive PROCESSOR (1st direction control node) has a connection to a SPIGOT (receive node) which is connected to a BUS SWITCH (1st direction control arrangement). An Arb is present in the BUS SWITCHs in which an inherent request to set up is made (send switching arrangement) and an inherent

response is setup (receive switch arrangement). A BUS SWITCH is a first direction control switch and another BUS SWITCH is a second direction control switch . The source PROCESSOR is the send node and the input to the send processor is the 2nd direction control node.

The primary reference does not expressly call for: TRI State drivers but teaches a shared bus.

Wang teaches: use of TRI state drivers per col. 1 lines 24-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the TRI State drivers of Wang to the system of the primary reference because TRI State drivers are utilized when multiple subsystems share the same bus.

Referring to Claim 12, The primary reference teaches the communications bus of claim 8 and A plurality of destination processors (receive and additional). The input of the destination PROCESSOR (1st direction control node) has a connection to a SPIGOT (destination node) which is connected to a BUS SWITCH (2nd direction control arrangement).

An Arb is present in the BUS SWITCHs in which an inherent request to set up is made (send switching arrangement) and an inherent response is setup (receive switch arrangement).

A BUS SWITCH is a first direction control switch and another BUS SWITCH is a second direction control switch . The source PROCESSOR is the send node and the input to the send processor is the 2nd direction control node.

The primary reference does not expressly call for: TRI State drivers but teaches a shared bus.

Wang teaches: use of TRI state drivers per col. 1 lines 24-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the TRI State drivers of Wang to the send and receive of the primary reference because TRI State drivers are utilized when multiple subsystems share the same bus.

Referring to Claim 17, The primary reference teaches the communications bus of claim 13 and A plurality of source processors (send and additional). The input of the destination PROCESSOR (2nd direction control node) has a connection to a SPIGOT (destination node) which is connected to a BUS SWITCH (2nd direction control arrangement).

An Arb is present in the BUS SWITCHs in which an inherent request to set up is made (send switching arrangement) and an inherent response is setup (receive switch arrangement).

A BUS SWITCH is a first direction control switch and another BUS SWITCH is a second direction control switch . The source PROCESSOR is the send node and the input to the send processor is the 2nd direction control node.

The primary reference does not expressly call for: TRI State drivers but teaches a shared bus.

Wang teaches: use of TRI state drivers per col. 1 lines 24-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the TRI State drivers of Wang to the send and receive of the primary reference because TRI State drivers are utilized when multiple subsystems share the same bus.

Claim Rejections - 35 USC § 103

5.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mostashari (U.S.

Patent No.: 4,964,120)

Referring to Claim 18, Mostashari teaches: Method for detection of faults between two TBC modules or source and destination nodes which have redundant cables (bus) and each of these redundant cables is utilized in token bus network therefore each of these cable or bus with alternate paths per col. 2 lines 5-44.

signals are applied to both cables between the two TBC modules or source and destination nodes per col. 2 lines 5-44 (Applying); A determination is made whether a valid signal received per col. 2 lines 5-44 (determining); If the same signal is not received then the TBC switch to an alternate cable (If test not properly received then switch paths)

Mostashari does not expressly call for: test signal but teaches sending the same signal down both cables per col. 2 lines 5-44.

It would have been obvious to one of ordinary skill in the art at the time of the invention that sending the same signal down both cables performs the same function as a test signal.

In Addition Mostashari teaches:

Regarding Claim 19, the reference teaches that the TBCs send same signal is sent down both cables or second test signal per col. 2 lines 5-44 (Applying); The reference teaches that a determination is made whether the signal is valid per col. 2 lines 5-44 (determining)

Regarding Claim 20, The reference teaches that the TBCs send same signal is sent down both cables or second test signal per col. 2 lines 5-44 (Applying); The reference teaches that a determination is made whether the signal is valid per col. 2 lines 5-44 (determining); If a valid signal is not received the TBC switches to the other cable per col. 2 lines 5-44 (If test signal not proper then switch)

Regarding Claim 21, The applicant broadly claims a "control signal". The examiner interprets the signal sent by the TBC as a control signal per col. 2 lines 5-44)

Regarding Claim 22, The reference teaches that the signal is sent from the Token Bus Controller or TBC. The examiner take official notice that it is well known in the art that a controller has memory. It would have been obvious to one of ordinary skill in the art at the time of the invention that the TBC which sends the signal would have a memory)

Claim Objections

6.0 Claim 5 is objected to because of the following informalities: Claim 5 depends upon itself. The examiner recommends that the applicant make the claim depend upon another claim. Appropriate correction is required.

Specification

7.0 The examiner objects to having the figure reference numbers in the abstract. The examiner requests that the figure reference numbers be deleted. Appropriate correction is required.

Conclusion

8.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571/272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
February 1, 2005

Chau T. Nguyen

CHAU NGUYEN
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